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Substitute for form 1449AVP10				Application Number	10/786,643	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT			SURE	Filing Date	February 25, 2004	
			CANT	First Named Inventor .	Cheng, et al.	
				Art Unit	TBD	
(Use as many sheets as necessary)			v)	Examiner Name	TBD	
Sheet	1	of	2	Attorney Docket Number	TSM03-0698	

	U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Document Number  Number - Kind Code <sup>2</sup> (************************************	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
W	1	US-2003/0162348 A1	08-28-2003	Yeo, et al.			
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FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No.1	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T	
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5.050			Application Number	10/786,643	
INI	FORMATION DISCL	OSURE	Filing Date	February 25, 2004	
STATEMENT BY APPLICANT  (Use as many sheets as necessary)		First Named Inventor	Chéng, et al.		
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		NON PATENT LITERATURE DOCUMENTS				
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M 2		Rim, K., et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's," IEEE Transactions on Electron Devices, vol. 47, no. 7, pp. 1406-1415, July 2000.				
	3	Rim, K., "Strained Si Surface Channel MOSFETS for High-Performance CMOS Technology," IEEE International Solid-State Circuits Conference, paper #7.3, pp. 116-117, 2001.				
	4	Yeo, Y.C., et al., "Enhanced performance in Sub-100 nm CMOSFETs using Strained Epitaxial Silicon-Germanium," International Electron Device Meetings, pp. 753-756, 2000.				
	5	Ootsuka, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meetings, pp. 575-578, 2000.				
	6	Ito, S., et al., "Mechanical Stress Effect of Etch-Stop Nitride and Its Impact on Deep Submicron Transistor Design," International Electron Device Meetings, pp. 247-250, 2000.	*			
	7	Shimizu, A., et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," International Electron Device Meetings, pp. 433-436, 2001.				
	8	Ota, K., et al., "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," International Electron Device Meetings, pp. 27-30, 2002.				
1	9	Scott, G., et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress," International Electron Device Meetings, pp. 827-830, 1999.				
KZ	10	Blanchi, R.A., et al., "Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance," International Electron Device Meetings, pp. 117-120, 2002.				
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